Yinxiao Feng

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PROFILE

I'm a fourth-year Ph.D. candidate at the Institute for Interdisciplinary Information Sciences (headed by Prof. **Andrew Chi-Chih Yao**), Tsinghua University (THU). I'm advised by assistant Prof. **Kaisheng Ma** and also work closely with Prof. **Dong Xiang**. My research interests lie in the fields of computer architecture and high-performance computing systems, including chiplet architectures, on/off-chip interconnection networks, distributed systems, and AI systems. I received my bachelor's and second bachelor's degrees at Shanghai Jiaotong University (SJTU).

EDUCATION

Institute for Interdisciplinary Information Sciences, THU — August 2020 - Present
Ph.D. candidate in Computer Science and Technology

School of Electronic Information and Electrical Engineering, SJTU — September 2016 - June 2020
Bachelor Degree of Information Engineering, GPA: 3.9/4.3

Zhiyuan College, SJTU — September 2016 - June 2020
Zhiyuan Honors Bachelor Degree of Engineering (Top 5% in SJTU)

School of Mathematical Sciences, SJTU — March 2018 - June 2020
The Second Bachelor Degree in Mathematics & Applied Mathematics

SELECTED PUBLICATIONS

MICRO-2023: Yinxiao Feng, Dong Xiang, Kaisheng Ma, "Heterogeneous Die-to-Die Interfaces: Enabling More Flexible Chiplet Interconnection Systems," 56th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), Toronto, ON, Canada, 2023.

HPCA-2023: Yinxiao Feng, Dong Xiang, Kaisheng Ma, "A Scalable Methodology for Designing Efficient Interconnection Network of Chiplets," 2023 IEEE International Symposium on High-Performance Computer Architecture (HPCA), Montreal, QC, Canada, 2023, pp. 1059-107.

DAC-2022: Yinxiao Feng, Kaisheng Ma, "Chiplet Actuary: A Quantitative Cost Model and Multi-chiplet Architecture Exploration," Proceedings of the 59th ACM/IEEE Design Automation Conference (DAC), New York, NY, USA, 2022, 121–126.

SELECTED PROJECTS

Wafer-based HPC interconnection network — May 2023 - Present
SC-2024
· under review

Ring Road: Polar-Coordinate-based NoC — May 2023 - Present
MICRO-2024
· under review

Parallel Simulator for Chiplet-based Networks — July 2022 - Present
ATC-2024
· under review

Heterogeneous Die-to-Die Interface — September 2022 - August 2023
MICRO-2023
· For multi-chiplet systems, we analyze the limitations of the uniform die-to-die interface and propose the *heterogeneous interface* architecture. We are the first to discuss the hetero-IF-based multi-chiplet architecture.

- We present two typical heterogeneous interface implementations: *Heterogeneous PHY (Hetero-PHY)* and *Heterogeneous channel (Hetero-Channel)*. The characteristics and usage of the two implementations are introduced. We also discuss the microarchitectures and overheads of the heterogeneous interface.
- We present hetero-IF-based multi-chiplet interconnection networks and give methods for applying deadlock-free routing and flexible scheduling. Evaluations show that the hetero-IF delivers huge performance and energy improvements under various workloads.

Scalable Chiplet Interconnection Architecture December 2021 - October 2022
HPCA-2023

- We present a method to scale large high-radix interconnection systems with 2D-mesh-NoC-based chiplets, achieving more efficient and flexible interconnection without changing much of the typical NoC architecture.
- We propose a scalable deadlock-free adaptive routing algorithm for interconnection networks of chiplets. The algorithm is applicable to most common topologies, including nD-mesh, hypercube, and dragonfly.
- We introduce the *safe/unsafe* flow control and the *network interleaving* method to address potential drawbacks arising from the new interconnection design. The two methods are general and can be applied to most multi-channel interconnection networks.
- We present a cycle-accurate C++ simulator called *CISim* designed specifically for multi-chiplet networks. The evaluation results show that our methodology has significant performance advantages over traditional multi-chiplet interconnection networks based on flat topologies.

Chiplet Acturay January 2021 - February 2022
DAC-2022

- We abstract monolithic SoC and multi-chip integration into different levels of concepts: module, chip, and package, by which we build a unified architecture.
- We present a quantitative cost model *Chiplet Actuary* to estimate various components of the total system cost. To the best of our knowledge, this model is the first to introduce D2D overhead and NRE cost.
- Based on *Chiplet Actuary*, we put forward an analytical method for decision-making on chiplet architecture problems: which integration scheme to use, how many chiplets to partition, whether to reuse packaging, how to leverage chiplet reusability, and how to exploit heterogeneity.

TEACHING

AI+X Computing Acceleration:
From Algorithm Development and Analysis to Actual Deployment Summer 2022 & 2023
Teaching Assistant (also give guest lectures)

Getting Started with Artificial Intelligence Chips:
From Hardware Description Languages to FPGA Implementations Fall 2021
Teaching Assistant (also give guest lectures)

HONORS & AWARDS

2023: Tsinghua University Scholarship (First Class)
2020: Outstanding Graduate of Shanghai
2019: National Scholarship
2015: First Prize in Chinese Physics Olympiad in Senior

STRENGTHS

I have a strong background in mathematics, computer science, and electronic engineering, especially chiplet architecture and on/off-chip interconnection networks. I'm also familiar with AI chips, high-performance computing, and distributed systems.

I have good C++/Python knowledge and experience in research and development. I'm also familiar with VLSI design and FPGA development by using Verilog.

I'm highly motivated, self-driven, and able to learn topics quickly. I can work independently or work as part of a team.

DECLARATION

I hereby declare that all the details furnished above are true to the best of my knowledge and belief.