YINXIAO FENG

Researcher / Engineer, ByteDance, Beijing, China
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EDUCATION

Institute for Interdisciplinary Information Sciences, Tsinghua University Aug. 2020 – Jun. 2025
Ph.D. Degree in Computer Science and Technology
Advisor: **Kaisheng Ma**, Associate Professor

School of Electronic Information and Electrical Engineering, Shanghai Jiaotong University Sept. 2016 – Jun. 2020
Bachelor's Degree in Information Engineering
Zhiyuan Honors Bachelor Degree in Engineering (Top 5% in SJTU)

School of Mathematical Sciences, Shanghai Jiaotong University Mar. 2018 – Jun. 2020
The Second Bachelor's Degree in Mathematics & Applied Mathematics

EXPERIENCE

ByteDance, Beijing Mar. 2025 - Present
Researcher / Engineer, working on *"AI Chip / System Architecture"*

Scalable Parallel Computing Laboratory (SPCL), ETH Zurich Jul. 2024 - Dec. 2024
Academic Guest, working on *"Interconnection Network Architecture for LLM Training"*
Host: **Torsten Hoefler**, Professor

HONORS & AWARDS

2025: Outstanding PhD Graduate of Tsinghua University (2 in IIIS, 112 in THU)
2025: Endeavor Scholarship - Talent for Integrated Circuit (8 in Tsinghua, 93 in China)
2024: ByteDance Scholarship (15 in China and Singapore)
2024: National Scholarship (2 of all CS PhD students in IIIS, THU)
2024: Social Work Excellence Scholarship of THU
2023: Integrated Circuit High-Level Urgently-Needed Talents (China Education Development Foundation)
2023: Comprehensive Excellence Scholarship of THU (First-Class)
2022: Comprehensive Excellence Scholarship of THU (Second-Class)
2020: Outstanding Graduate of Shanghai
2019: National Scholarship (Undergraduate)
2018: Meritorious Winner in Mathematical Contest in Modeling
2018: Huawei Scholarship of SJTU
2017: Three-Good Student of SJTU
2015: First Prize in Chinese Physics Olympiad in Senior

SELECTED PUBLICATIONS

Yinxiao Feng and Kaisheng Ma. 2022. Chiplet Actuary: A Quantitative Cost Model and Multi-Chiplet Architecture Exploration. In *59th ACM/IEEE Design Automation Conference (DAC)*, ACM, San Francisco, CA, USA, 121–126. https://doi.org/10.1145/3489517.3530428 (CCF-A)

Yinxiao Feng and Kaisheng Ma. 2024. Switch-Less Dragonfly on Wafers: A Scalable Interconnection Architecture Based on Wafer-Scale Integration. In *SC24: International Conference for High-Performance Computing, Networking, Storage, and Analysis*, IEEE, Atlanta, GA, USA, 1-17. https://doi.org/10.1109/SC41406.2024.00102 (CCF-A)

Yinxiao Feng, Dong Xiang, and Kaisheng Ma. 2023. A Scalable Methodology for Designing Efficient Interconnection Network of Chiplets. In *2023 IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, IEEE, Montreal, QC, Canada, 1059-1071. https://doi.org/10.1109/HPCA56546.2023.10070981 (CCF-A)

Yinxiao Feng, Wei Li, and Kaisheng Ma. 2024. Ring Road: A Scalable Polar-Coordinate-Based 2D Network-on-Chip Architecture. In *57th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, IEEE, Austin, TX, USA, 871-884. https://doi.org/10.1109/MICRO61859.2024.00069 (CCF-A)

Yinxiao Feng, Dong Xiang, and Kaisheng Ma. 2023. Heterogeneous Die-to-Die Interfaces: Enabling More Flexible Chiplet Interconnection Systems. In *56th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, ACM, Toronto, ON, Canada, 930–943. https://doi.org/10.1145/3613424.3614310 (CCF-A)

Yinxiao Feng, Yuchen Wei, Dong Xiang, and Kaisheng Ma. 2024. Evaluating Chiplet-Based Large-Scale Interconnection Networks via Cycle-Accurate Packet-Parallel Simulation. In *2024 USENIX Annual Technical Conference (ATC)*, USENIX Association, Santa Clara, CA, USA, 731–747. https://www.usenix.org/conference/atc24/presentation/feng-yinxiao (CCF-A)

TEACHING

AI+X Computing Acceleration:
From Algorithm Development and Analysis to Actual Deployment Summer 2022 & 2023
Teaching Assistant (also give guest lectures)

Getting Started with Artificial Intelligence Chips:
From Hardware Description Languages to FPGA Implementations Fall 2021
Teaching Assistant (also give guest lectures)

OTHER PUBLICATIONS

Zhenhua Wu, **Yinxiao Feng**, Yan Liu, Huilie Shi, Shuai Zhang, Zekun Liu, and Zhiyu Hu. 2021. Bipolar Resistive Switching in the Ag/Sb_2Te_3/Pt Heterojunction. in *ACS Applied Electronic Materials* 3 (6), 2766-2773. https://doi.org/10.1021/acsaelm.1c00341

Qichao Ma, **Yinxiao Feng**, and Kaisheng Ma, 2021. A Low-Power Ultra-Compact ultrasonic Communication System for Neural Spike Events Recording. in 2021 IEEE International Ultrasonics Symposium (IUS), IEEE, Xi'an, China, 1-4. https://doi.org/10.1109/IUS52206.2021.9593446